THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 29

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte MASAYA KITAGAWA

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Appeal No. 97-0320
Application 08/096,261[1]

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HEARD: March 11, 1999

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Before KRASS, JERRY SMITH, and RUGGIERO, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 and 3, which constitute all of the claims in the application. Claim 2 has been canceled. An amendment after

[1] Application for patent filed July 26, 1993.

final rejection was filed on September 8, 1995 and was entered by the Examiner. A further amendment after final rejection filed December 8, 1995 was also entered by the Examiner.

The claimed invention relates to a semiconductor memory device having a redundant circuit and a diagnostic circuit for carrying out a memory test to detect positions of defective memory cells. Further included is a defective cell position storage circuit and an output circuit for converting the defective cell position information into serial data.

Representative claim 1 is reproduced as follows:

1. A semiconductor memory device, comprising:

a normal memory portion having a memory cell matrix which is composed of a plurality of memory cells arranged at intersections of word lines and bit lines;

a redundant circuit means having memory cell arrays and operably coupled to said normal memory portion for replacing defective memory cells of said normal memory portion in a form such that all memory cells connected to the word line or the bit line to which a defective memory cell is connected are replaced;

a self-diagnostic circuit means, operably coupled to said normal memory portion, for testing whether or not all memory cells operate normally;

a defective cell position storage circuit means, operably coupled to said self-diagnostic circuit means, for storing a position of either a word line or a bit line connected to defective memory cells when said self-diagnostic circuit means

detects defective memory cells; and

an output circuit means, operably coupled to said defective cell position storage circuit means, for converting position information indicating positions of said word lines or bit lines connected to said defective memory cells stored in said defective cell position storage circuits into serial data and for outputting converted position information so that said positions of said word lines or bits connected to said defective memory cells can be determined and thereafter replaced.

The Examiner relies on the following references:

Müller et al. (Müller)	5,123,016	Jun. 16, 1992
Mizuno et al. (Mizuno)	5,357,473 (effectively filed Jun. 20, 1991)	Oct. 18, 1994

Claims 1 and 3 are rejected under 35 U.S.C. § 103 as being unpatentable over Müller in view of Mizuno.

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the Briefs[2] and Answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on

[2] The Appeal Brief was filed February 8, 1996. In response to the Examiner's Answer dated March 19, 1996, a Reply Brief was filed May 20, 1996 which was acknowledged and entered by the Examiner without further comment on July 29, 1996.

appeal, the rejection advanced by the Examiner and the evidence of obviousness relied upon by the Examiner as support for the rejection. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellant's arguments

set forth in the Briefs along with the Examiner's rationale in support of the rejection and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the obviousness of the invention as set forth in claims 1 and 3. Accordingly, we affirm.

As a general proposition in an appeal involving a rejection under 35 U.S.C. § 103, an Examiner is under a burden to make out a prima facie case of obviousness. If that burden is met, the burden of going forward then shifts to the Appellant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992); In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976). Only those arguments actually made by

Appellant have been considered in this decision.

Arguments which Appellant could have made but chose not to make in the Briefs have not been considered. See 37 CFR § 1.192(a).

With respect to claim 1, the Examiner has pointed out the teachings of Müller and Mizuno, has pointed out the perceived differences between this prior art and the claimed invention, and has reasonably indicated how and why Müller and Mizuno would have been modified and/or combined to arrive at the claimed invention. In our view, the Examiner's analysis is sufficiently reasonable that we find that the Examiner has satisfied the burden of presenting a prima facie case of obviousness. That is, the Examiner's analysis, if left unrebutted, would be sufficient to support a rejection under 35 U.S.C. § 103. The burden is, therefore, upon Appellant to come forward with evidence or arguments which persuasively rebut the Examiner's prima facie case of obviousness. Appellant has presented several substantive arguments in response to the Examiner's rejection. Therefore, we consider obviousness based upon the totality of the evidence and the relative persuasiveness of the arguments.

Appellant initially attacks the Examiner's combination of

Müller and Mizuno by asserting lack of motivation for the skilled artisan to look to Mizuno to supplement the teachings of Müller (Brief, page 10). In Appellant's view, Müller's provision of a memory fault identification feature negates the need to look to Mizuno for this teaching. The Examiner, however, has cited Mizuno for the sole purpose of providing a teaching of outputting defective cell position data in serial form (Answer, pages 3-5). The fact that a particular prior art reference may teach features which overlap the teachings of another reference does not devalue its use in supplementing features which may be lacking in such other reference.

In an analogous argument, Appellant submits (Brief, pages 11 and 12) that, since Müller provides for the output of a memory repair strategy to an external programming means, the addition of Mizuno's teaching of rewriting of the defective memories from outside the memories is superfluous. After careful review, however, it is our view that Appellant has misinterpreted the description of the operation of the system of Müller. It is clear that Müller's disclosure provides for alternative execution procedures for the memory repair strategy, i.e. either internally or externally. The Müller

reference at column 8, lines 18-24 states:

> When, by contrast, it is repairable, then the memory module can be repaired according to the repair plan (Step 10), whereby the repair can ensue externally or internally with the test processor when the replacement rows or replacement columns are programmable by the test processor.

Thus, while a portion of Müller's disclosure (column 3, lines 10-14) indicates a preference for internal repair with the test processor, an external repair alternative is clearly contemplated. We do note, as the Examiner does, that Mizuno does not explicitly disclose any particular output circuitry such as the presently claimed output data serialization feature for implementing such external repair procedure. It is precisely this deficiency, however, that the Examiner seeks to address with the addition of Mizuno. The Examiner points to the disclosure of Mizuno (column 10, lines 59-68 and Figure 3) which describes the output of memory defect data through a serial port to an external computer 17 which in turn executes the memory repair. The Examiner (Answer, pages 3 and 4), suggests several advantages of off-chip memory defect analysis and repair and concludes that one of ordinary skill would have

been motivated to add an output data serialization feature as taught by Mizuno to Müller to implement Müller's alternative external repair procedure. We agree with the Examiner that a skilled artisan would have found obvious the addition to Müller of an output data serialization feature in view of the serial port and external computer memory repair disclosure of Mizuno.

Appellant further asserts at pages 14 and 15 of the Brief that even assuming, arguendo, the appropriateness of the Examiner's proposed combination, such combination would still fall short of meeting the claimed invention. Although Appellant, in making this argument, suggests in general terms that the Examiner has not established the existence in the references of all of the claimed elements, Appellant's primary contention centers on the deficiencies of the references in disclosing the claimed output circuit. The relevant portion of Appellant's claim 1 recites:

> an output circuit means, operably coupled to said defective cell position storage circuit means, for converting position information indicating positions of said word lines or bit lines connected to said defective memory cells stored in said defective cell position storage

> circuits into serial data and for outputting converted position information so that said positions of said word lines or bits connected to said defective memory cells can be determined and thereafter replaced.

As discussed earlier, in addressing this claimed feature, the Examiner (Answer, page 3) has relied on Mizuno's description of the connection of the memory repair system through a serial port 15 to an external computer 17. In response to the Examiner's arguments, Appellant contends (Reply Brief, pages 8 and 9) that In re Donaldson Co., 16 F. 3d 1189, 1193, 29 USPQ2d 1845, 1848 (Fed. Cir. 1994) requires that the "means for" language occurring in the claims, in accordance with 35 U.S.C. § 112, sixth paragraph, must be interpreted as covering the structure, material or acts set forth in the specification and equivalents thereof. We note that, since the Reply Brief was entered without further response by the Examiner, we do not have the benefit of the Examiner's comments on this particular argument of Appellant. However, it is our view that, while Appellant has pointed to corresponding structure within their specification for the "output circuit" means statement in the claim, from our earlier discussion we are not

persuaded that the structure disclosed by Mizuno would not be considered equivalent. Clearly, the data serialization process required by the serial port connection in Mizuno would necessarily include appropriate logic and timing circuitry.

In a related argument, Appellant asserts (Brief, page 18; Reply Brief, page 8) that Mizuno provides only for the rewriting of defective memory cells from the external computer 17 through the serial port to the memories but has no disclosure of defective memory cell information being output through the serial port to the external computer. In response, the Examiner argues (Answer, page 6) that the defective memory cell information required by the external computer 17 in Mizuno to rewrite the defective memories must be output to the computer through the serial port since no other connection is shown. After careful review of Appellant's arguments and the Mizuno reference, we are in agreement with the Examiner. In our view, the conclusion that Mizuno's computer 17 receives required information from any other source or connection other than that shown is not supported by any showing by Appellant. For the above reasons, the Examiner's rejection of claim 1 under 35 U.S.C. § 103 as

unpatentable over Müller in view of Mizuno is sustained.

With respect to claim 3, Appellant has indicated (Brief, page 7) that claims 1 and 3 do not stand and fall together. We note, however, that Appellant's arguments with regard to claim 3 are directed to the same claim limitations as appear in claim 1. Since we have previously determined that the arguments with respect to claim 1 are not persuasive of error by the Examiner, and since Appellant makes no additional arguments with respect to claim 3, we also sustain the rejection of claim 3 under U.S.C. § 103.

For all of the above reasons, the decision of the Examiner rejecting claims 1 and 3 under 35 U.S.C. § 103 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

ERROL A. KRASS Administrative Patent Judge	)	
JERRY SMITH Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
JOSEPH F. RUGGIERO Administrative Patent Judge	)	

JFR:svt

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